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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,426	06/19/2001	Daniel Sobek	AMD-E306	4225

7590 11/20/2002  
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EXAMINER

VU, QUANG D

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/885,426

Applicant(s)

SOBEK ET AL.

Examiner

Quang D Vu

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08/21/2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 14-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other:

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 16-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16, in lines 1-2, the phrase "...prior to said forming a bitline a polysilicon layer is formed over said gate" is unclear. The specification discloses forming the polysilicon layer (311) on the ONO (302) (figure 4). Then, the polysilicon layer (311) is formed as the part of the gate (figure 7). The specification never discloses forming the polysilicon (311) over the gate.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 14-15 and 19-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,477,084 to Eitan in view of US Patent No. 5,879,990 to Dormans et al.

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Regarding claim 14, Eitan (figures 7A-F) teaches a process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:

forming a gate (112) above the channel of the substrate (166);

forming a bitline (104).

Eitan teaches the bitline (104) is the drain (column 6, lines 28-29).

Eitan differs from the claimed invention by not siliciding the bitline. However, Dormans et al. teach siliciding (26) the source/drain (11 and 12) (figures 7-8; column 5, lines 22-28) in a non-volatile memory cell. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Dormans et al. into the method taught by Eitan, since the silicide layers reduce the resistivity of the source/drain.

Regarding claim 15, Eitan teaches forming an oxide (178) (column 9, lines 56-57) over the silicided bitline (104).

Regarding claim 19, Eitan teaches electron jump into the nitride layer (110) by hot electron injection (column 2, lines 11-17). Eitan also teaches forming a charge-stored region (162) that contains a first amount of charge; and forming a layer (160) between the channel and the charge-stored region (162), wherein the layer (162) has a thickness (column 7, line 64 – column 8, line 4). Eitan does not disclose forming a layer between the channel and the charge-trapping region, wherein the layer has a thickness such that the first amount of charge is prevented from directly tunneling into the layer. It is inherent that the first amount of charge is prevented from directly tunneling into the layer because the first amount of charge (electron) jumps into the charge storage region by hot electron injection.

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Regarding claim 20, Eitan teaches the charge trapping region (162) comprises nitride (column 7, lines 64-65). It is inherent that the nitride is silicon nitride.

Regarding claim 21, Eitan differs from the claimed invention by not showing the gate comprises an N-type material. However, Dormans et al. teach the gate layer (17) comprises an N-type material (column 4, lines 39-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Dormans et al. into method taught by Eitan, since it reduces the resistance of the gate electrode.

Regarding claim 22, Eitan differs from the claimed invention by not showing the gate comprises a polycrystalline silicon. However, Dormans et al. teach the gate comprises a polycrystalline silicon (column 4, lines 39-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Dormans et al. into method taught by Eitan, since it reduces the resistance of the gate electrode.

Regarding claim 23, Eitan teaches forming an insulating layer (164) on the charge trapping region (162) (figures 7A-F).

Regarding claim 24, Eitan teaches the insulating layer (164) comprises oxide (column 7, lines 64-65) (figures 7A-F). It is inherent that the oxide is silicon dioxide.

Regarding claim 25, Eitan teaches the charge trapping region (162) comprises nitride (column 7, lines 64-65). It is inherent that the nitride is silicon nitride.

Regarding claim 26, Eitan teaches the memory cell comprises an EEPROM memory cell (column 1, lines 9-12).

Regarding claim 27, Eitan teaches the memory cell comprises a two-bit memory cell (a left bit [102] and a right bit [104]) (column 6, lines 28-29; column 8, lines 33-34).

Regarding claim 28, Eitan teaches the substrate comprises a P-type substrate (column 8, lines 1-3).

Regarding claim 29, Eitan differs from the claimed invention by not showing the process further comprising scaling the length of the bitline. It would have been ordinary skill in the art at the time the invention was made to scale the length of the bitline, since it has been held that discovering an optimum value of a result effect variable involves only routine skill the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 30, Eitan differs from the claimed invention by not showing the scaling comprises reducing the thermal cycle of the bitline. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the bitline by thermal process, since it is a well known process to reduce or increase the length of the bitline.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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QV  
November 18, 2002

*Steven Loh*